TOWARDS HIGHLY EFFICIENT MONOLITHIC DC/DC CONVERTER

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Outline

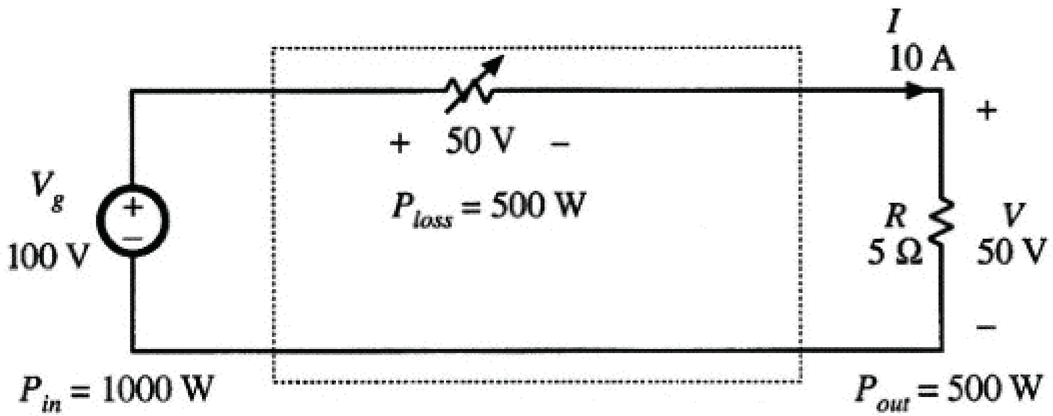
- Introduction
- Types of Switching Regulators
  - Buck Converter
  - Modes of operation of Buck converter
  - Boost converter
- Structure of monolithic Converter
- Method of operation of various parts of the converter.
- Integration of Inductor on chip
- Integration of capacitor on chip
- Power losses in the converter
- Power flow analysis
- Issues in monolithic DC/DC converter
- Techniques to improve performance
  - Compensated Error amplifier
  - Light load efficiency

What is DC/DC Converter?

- A device that accepts a DC input voltage
- Produces a DC output voltage
- **Used to provide:**
  - Noise isolation
  - Power bus regulation etc.
  - Output at different voltage level
  - Wide Input voltage range
  - Constant Output Voltage
  - Galvanic Isolation

Linear Regulator

- Extremely inefficient (depending on voltage drop!)
- High heat dissipation
- Bulky and expensive heat sink
- Impossible for SOC design
- Reduce battery life
- No switching noise



Switching Regulator

- Takes small chunk of energy from i/p & transfer to the o/p
- Uses electrical switch & controller to regulate rate of energy
- High efficiency
- Used in portable devices- cell phones, laptops, robots etc.
- Smaller size
- Lower heat generation
- Suitable for on chip design

Disadvantages of Switching Regulator

- Complex System Design
- High frequency electrical noise
- Ripple voltage at switching frequency

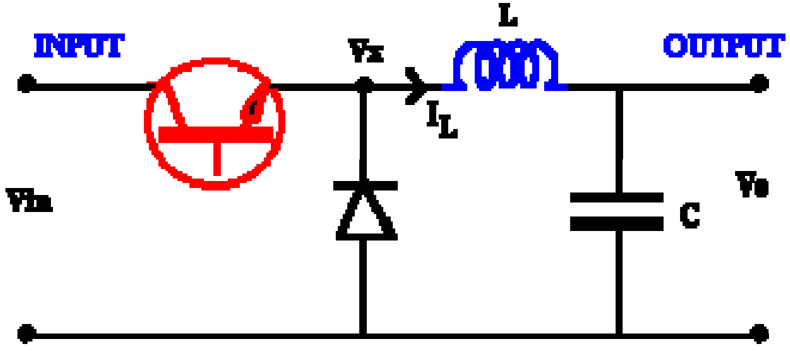


Fig. Buck Converter.

Types of Switch Mode Regulators

- Buck Converter- Step-down converter
- Boost Converter- Step-up converter
- Cuk Converter
- Isolated converters:
    - Flyback converter
    - Forward converter
    - Full- / Half bridge converter

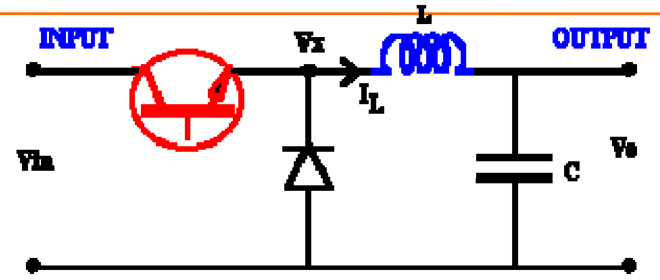


Fig. Buck Converter.

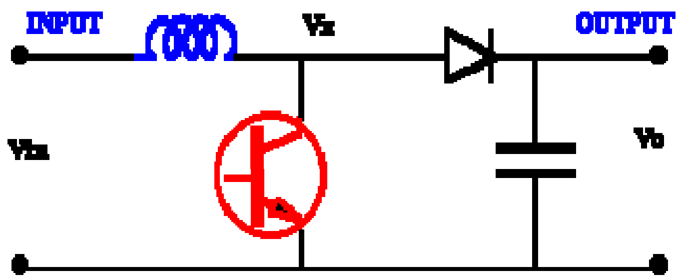


Fig. Boost Converter.

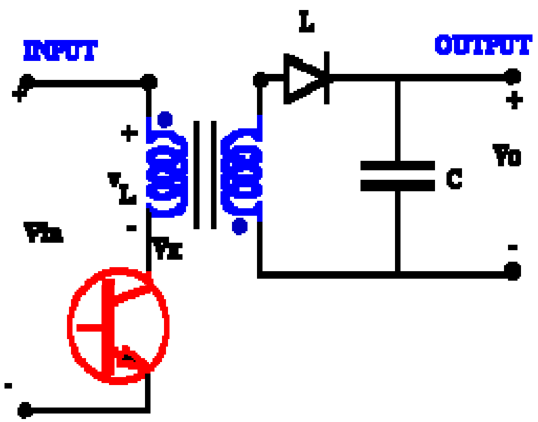


Fig. Flyback Converter.

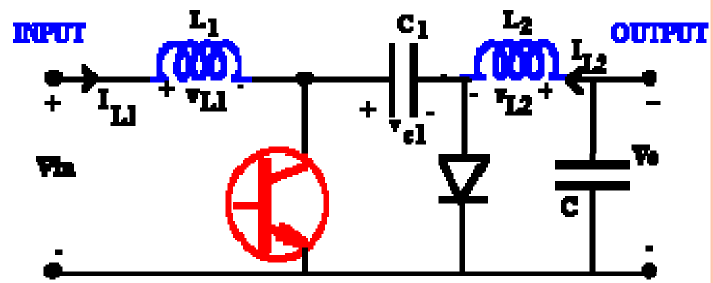


Fig. Cuk Converter.

Buck Converter

When Transistor 'ON'

- ❑ Inductor current rises

When Transistor 'OFF'

- ❑ Current through inductor passes through the diode

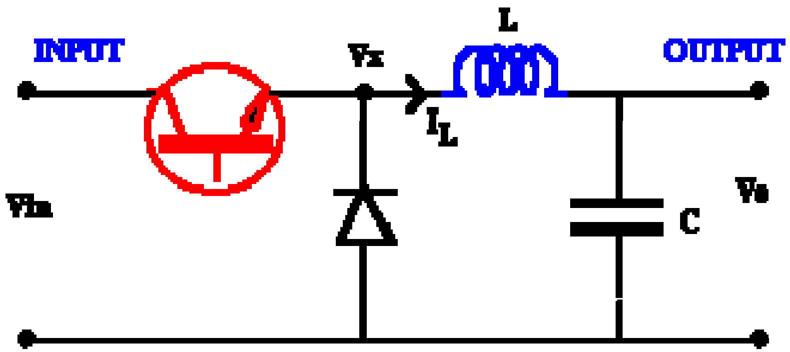


Fig. Circuit Layout Of Buck Converter

Modes of operation:

- ❑Continuous Mode
- ❑Transition b\w Continuous & Discontinuous Mode
- ❑Discontinuous Mode

Continuous Mode

Now, $Vx - Vo = L\frac{di}{dt}$

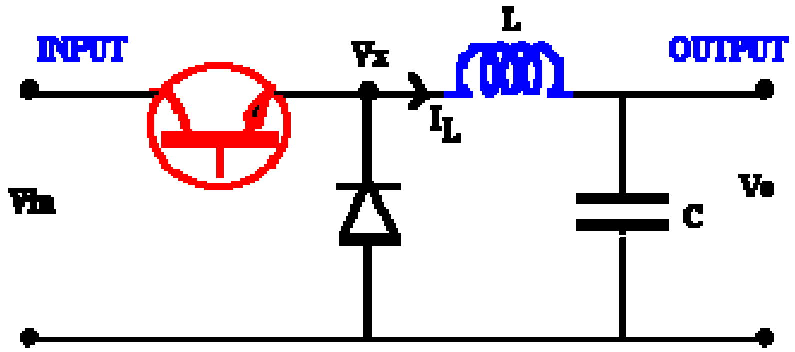
The change in current satisfies,

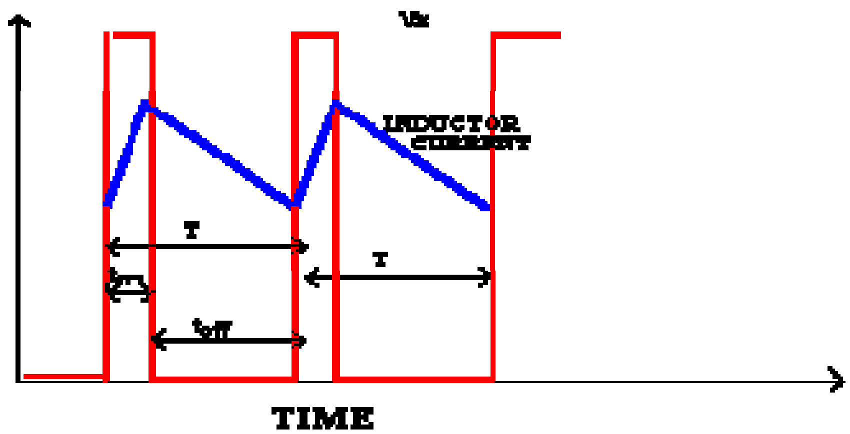
$$di = \int_{ON} (Vx - Vo)\,dt + \int_{OFF} (Vx - Vo)\,dt$$

For steady state operation,

$$di = 0 = \int_{ON} (Vx - Vo)\,dt + \int_{OFF} (Vx - Vo)\,dt$$

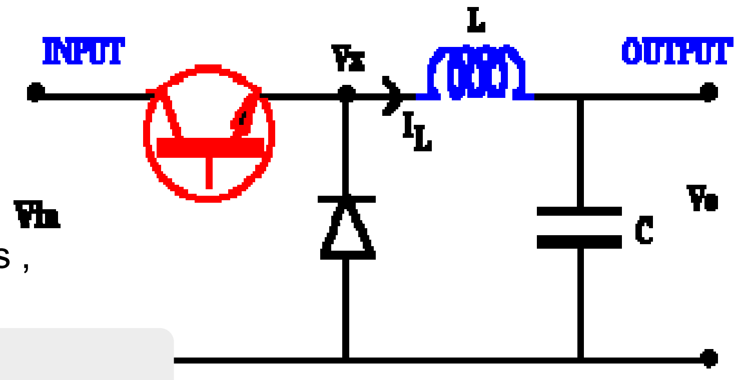
Hence, $\frac{Vo}{Vin} = \frac{ton}{T}$





Transition b\w Continuous & Discontinuous Mode

- Inductor current just goes to zero.

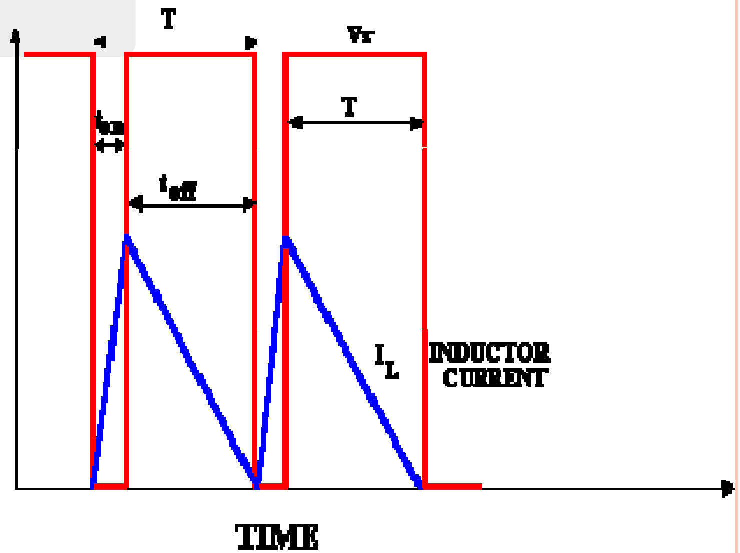


Now, during the ON time V_{in} - V_{out} is across the inductor thus,

$$I_L(peak) = (Vin - Vout)\frac{t_{ON}}{L}$$

The average current which must match the output current satisfies ,

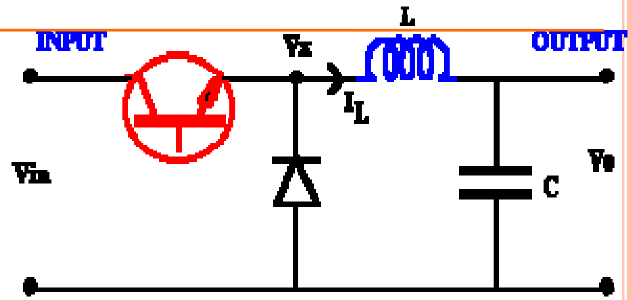
$$I_L(average\ at\ transition) = \frac{I_L(peak)}{2} = (Vin - Vout)\frac{dT}{2L} = I_{out}(transition)$$



Where, duty ratio, $d = \frac{t_{ON}}{T}$

the output current at the transition point satisfies,

$$Iout(transition) = Vin\frac{(1-d)d}{2L}T$$



Discontinuous Mode

- Transistor OFF time divided into :
  - segments of diode conduction d_dT and
  - zero conduction d_oT.
- The inductor average voltage gives ,

$$(Vin - Vo)dT + (-Vo)\delta_d T = 0$$

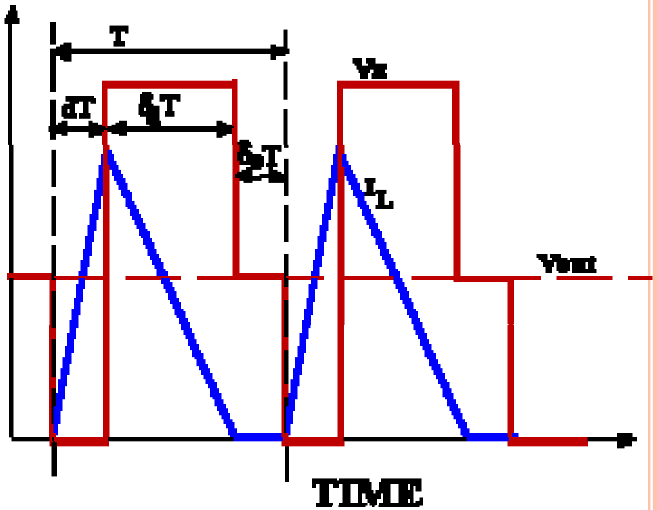
$$\frac{Vout}{Vin} = \frac{d}{d + \delta_d} \quad \text{--(1)}$$

- To resolve the value of consider the output current,

$$Iout = \frac{I_L(peak)}{2} d + \delta_d$$

- the change of current during the diode conduction time ,

$$I_L(peak) = \frac{Vo(\delta_d T)}{L}$$



Thus, from above equation

$$Iout = \frac{Vo\delta_d T(d + \delta_d)}{2L}$$

using the relationship in (1) ,

$$Iout = \frac{Vin\ d\ \delta_d T}{2L}$$

Discontinuous Mode

- Solving for the diode conduction , $\delta_d = \frac{2L\, Iout}{Vin\, d\, T}$

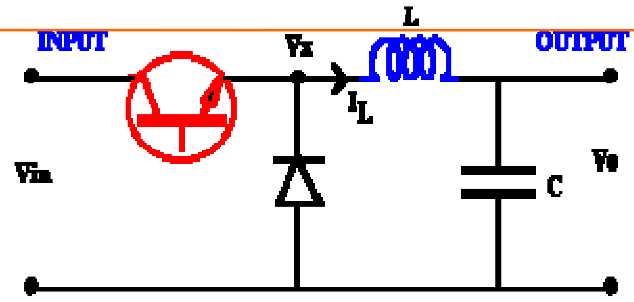
- The output voltage is thus given as ,

$$\frac{Vout}{Vin} = \frac{d^2}{d^2 + \left(\frac{2L\, Iout}{Vin\, T}\right)}$$

- defining k* = 2L/(V_{in} T),

- **Output voltage vs. Current**

  - High O/p current ➡ voltage ratio depends on the duty ratio "d".
  - Low currents ➡ discontinuous operation tends to increase o/p voltage of the converter towards V_{in}.



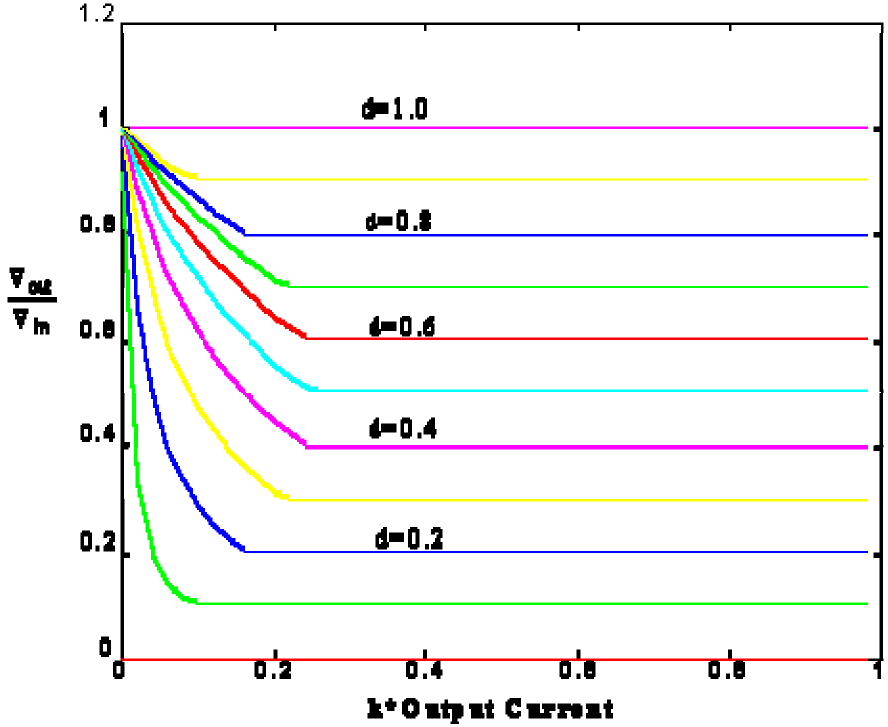


Fig. Output Voltage vs Current

- **When Transistor "ON"**
  - $V_x = 0$
- **When Transistor "OFF"**
  - $V_x = V_o$
- **For Steady State**

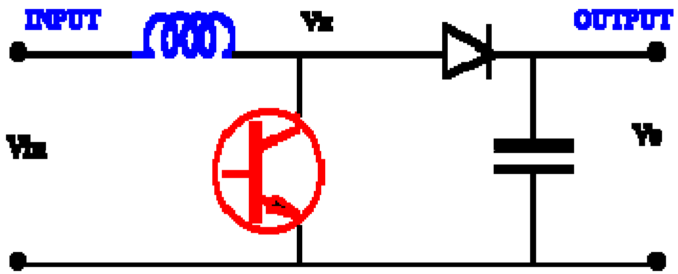


Fig. Boost Converter Circuit.

  - Voltage across the inductor & average must be zero for the average current.

$$Vin\, t_{on} + (Vin - Vo)\, t_{off} = 0$$

  - This can be rearranged to give,

$$\frac{Vo}{Vin} = \frac{T}{t_{off}} = \frac{1}{(1-D)}$$

- Since, the duty ratio "D" is b/w 0 and 1 ⇨ The output voltage must always be higher than the input voltage in magnitude.

Buck-Boost converter

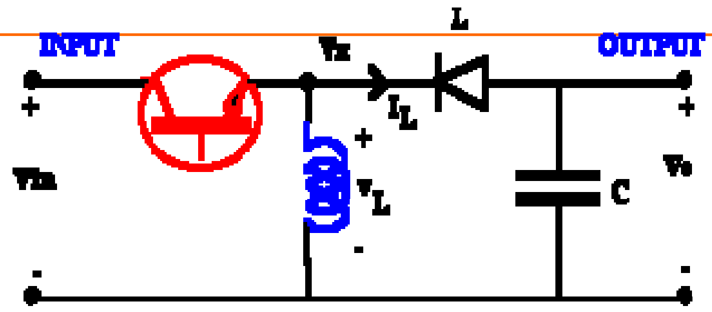


Fig. Buck-Boost Converter Circuit.

- **When Transistor "ON"**
  - $V_x = V_{in}$
- **When Transistor "OFF"**
  - $V_x = V_o$
- **For Steady State**
  - Voltage across the inductor & average must be zero for the average current.

$$Vin\ t_{ON} + Vo\ t_{OFF} = 0$$

  - This can be arranged to give voltage ration as,

$$\frac{Vo}{Vin} = -\frac{D}{(1-D)}$$

- Since, the duty ratio "D" is between 0 and 1 ➡ The output voltage may be higher or lower than the input voltage in magnitude.

Comparison Of Different Converters

- only the buck converter shows a linear relationship.
- The buck-boost can reduce or increase the voltage ratio with unit gain for a duty ratio of 50%.
- **Buck converter:** $\frac{Vo}{Vin} = \frac{ton}{T}$
- **Boost Converter:** $\frac{Vo}{Vin} = \frac{T}{t_{off}} = \frac{1}{(1-D)}$
- **Buck-Boost Converter:** $\frac{Vo}{Vin} = -\frac{D}{(1-D)}$

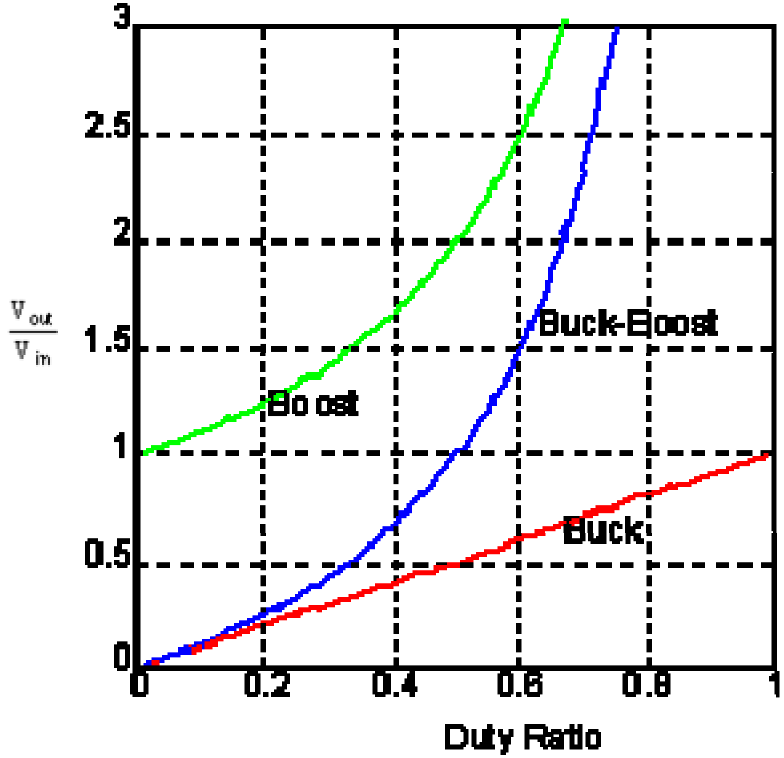


Fig. Comparison Of Voltage Ratio.

Monolithic Integrated DC/DC Converters

Why Monolithic DC/DC Converter?

- Required for portable devices-laptops, mobiles etc.
- Decrease the size & weight of these devices.
- Miniaturization of the power modules.
- Integrating a DC-DC converter can potentially lower the parasitic losses as interconnect b/w DC-DC converter & microprocessor is reduced.

- Need for on chip, point-of-load (PoL) power conversion.

Challenges

- Tight area constraint for the on-chip integration of inductive & capacitive elements.
- Poor parasitic impedance characteristics.
- High frequency ⟶ low value & physical size of passive devices required.

Applications

- Battery operated portable electronic devices like Laptops, cell phones, PDAs (Personal digital assistants) & other palm devices.

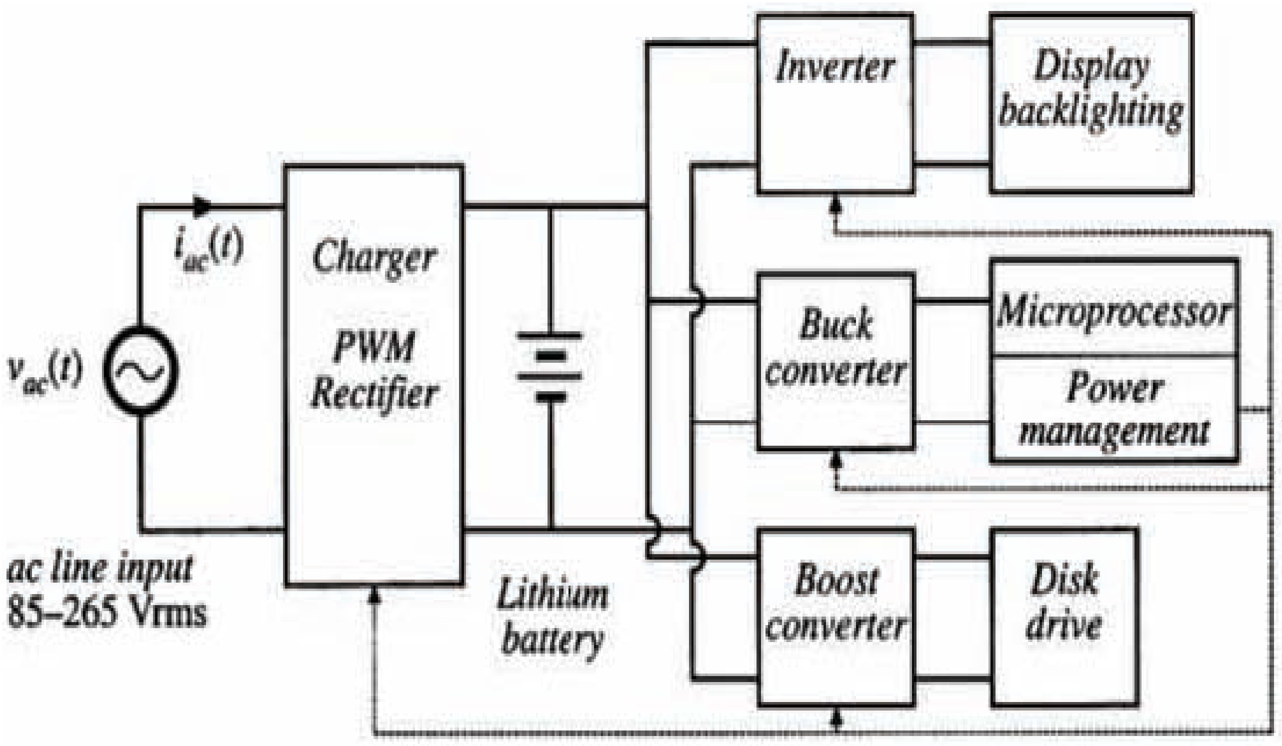


Fig. Laptop Computer power supply system.

Components

- Power Stage
- Compensator
- Modulator
- Voltage to current converter
  - Sensed Inductor Signal
  - Ramp signal
- Oscillator & ramp generator
- Pulse width generator
- Buffer

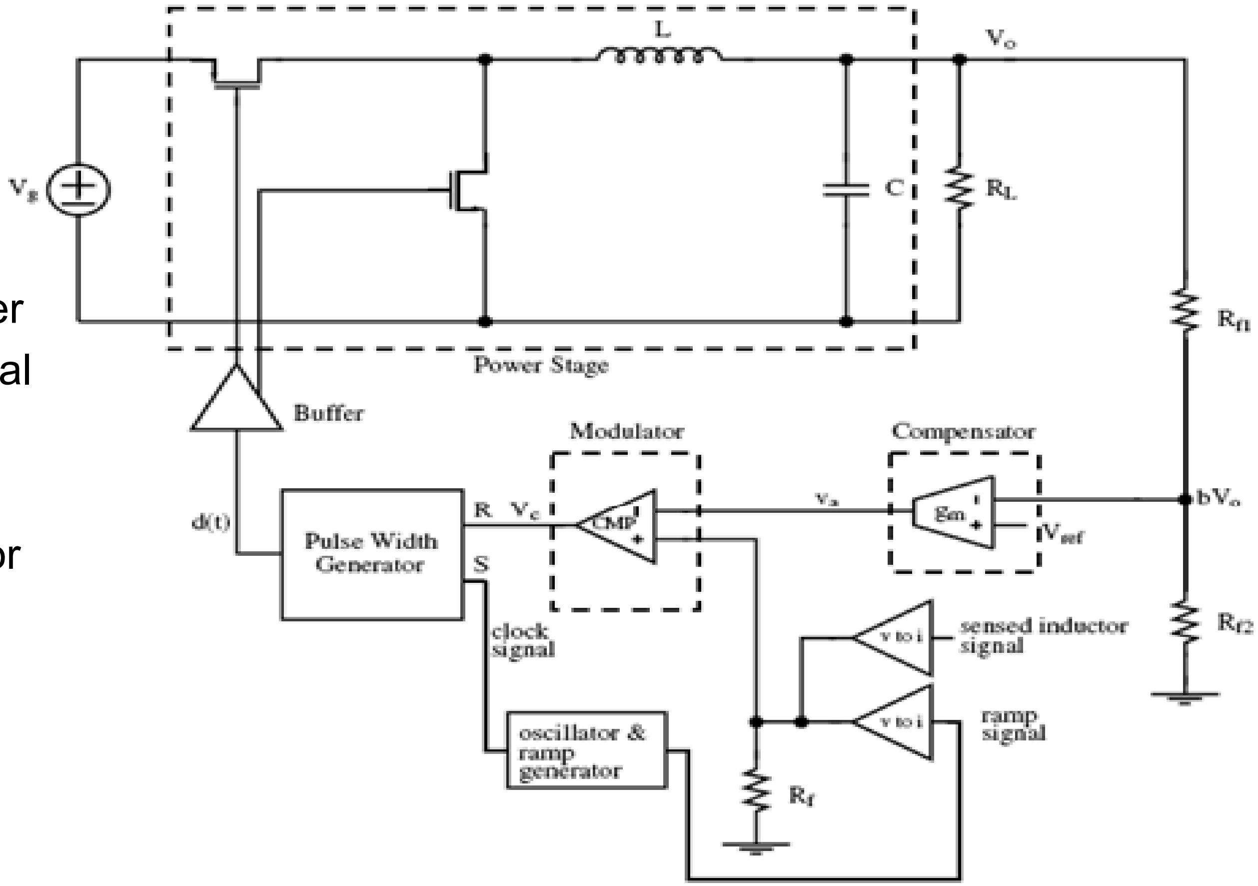


Fig. Structure of a Current Mode Buck Converter.

Power stage: Inductors for On Chip DC/DC Converter (MHz Frequency)

- MEMS based inductors.
- Use iron-based alloy plated on Si substrate.
- Is a metal slab completely encapsulated by a magnetic material.
- Spirals made of 1µm Al-Cu isolated from ground plane by 0.5 µm of SiO_2.
- The magnetic film surrounding metal is amorphous CoZrTa alloy that exhibits:-
  - small hysteresis losses.
  - Withstand temperature up to 450°C.
  - Integrated in standard high temperature CMOS Si process.
  - Cut off frequency of approx. 1.4GHz.

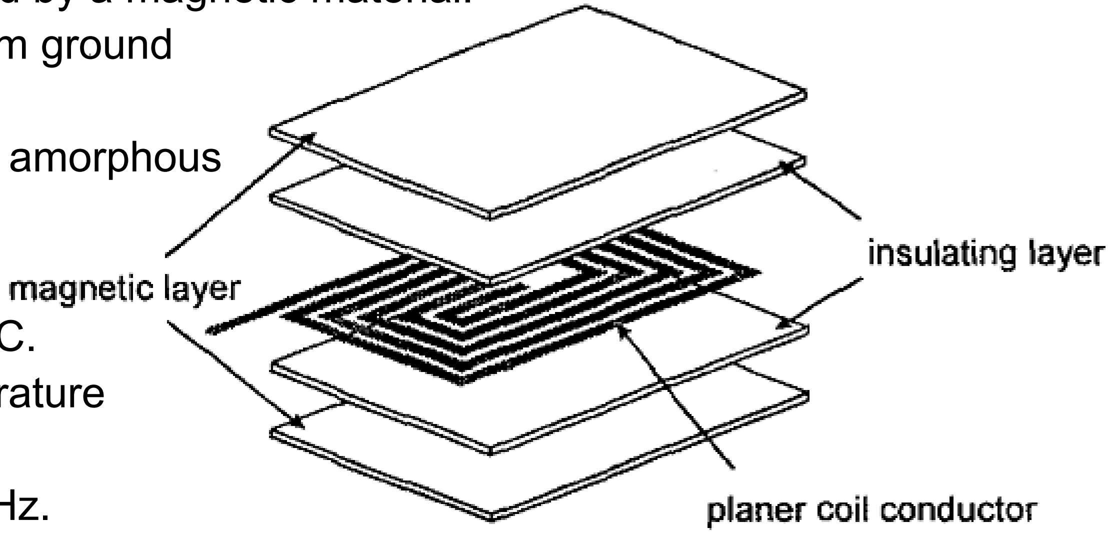
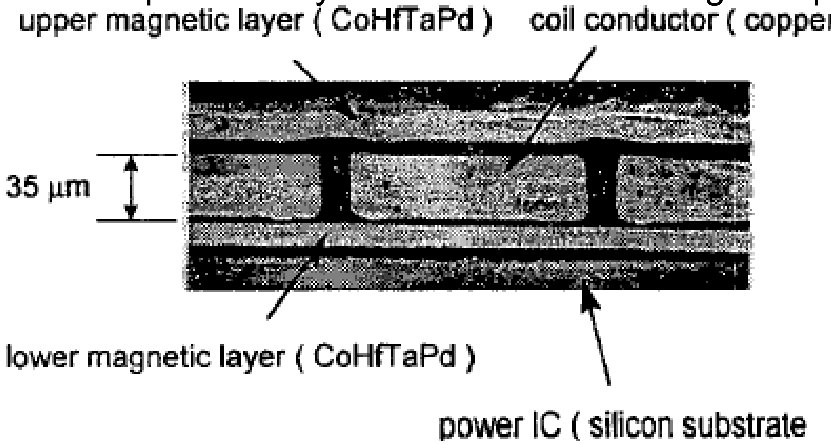


Fig. Schematic of Thin File Inductor.

- Superior higher frequency & saturation characteristics.
- Reduces size & parasitic effects.
- Performs at frequency up to & beyond 10 MHz.
- Magnetic material below & above spirals prevent straying of magnetic flux.
- One layer of magnetic material increases inductance by 36-50% & two layers by 100-500%.

Power stage: Inductors for On Chip DC/DC Converter (MHz Frequency)

- CoHfTaPd – Co based amorphous alloy can also be used at high frequency (few MHz) .



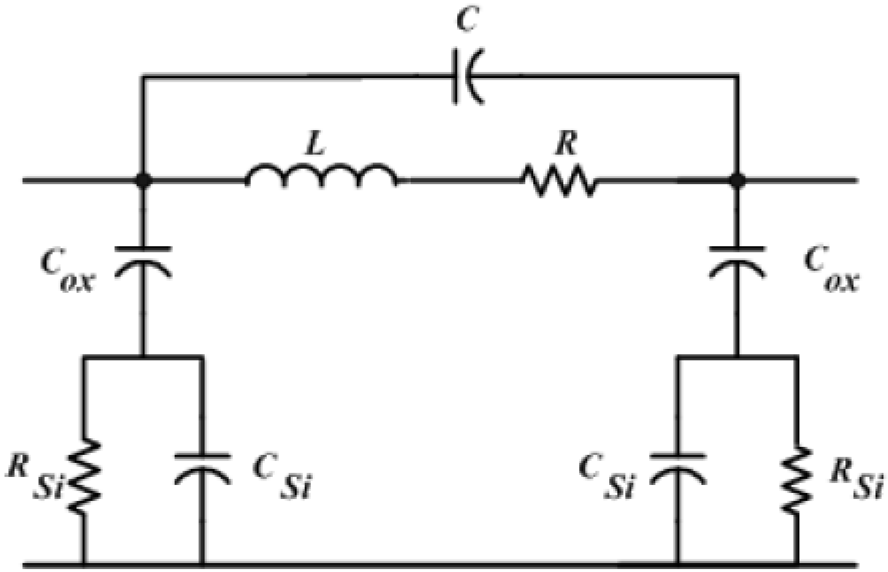


Fig. Circuit model of single layer spiral circuit

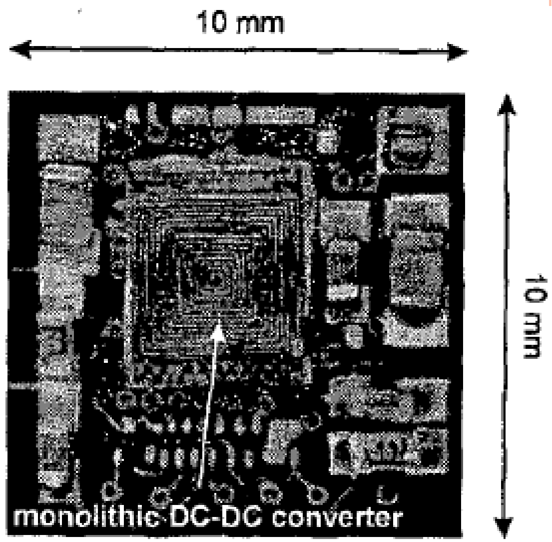


Fig. Top view of monolithic DC-DC converter. Size of inductor (4mm 4mm)*

Power Stage:Capacitors for On Chip DC/DC Converter (MHz frequency)

- Limited area overhead → Filter Capacitance integrated on a Microprocessor die is limited.
- Ranges between 100nF – 1nF.
- As Capacitance (↓) → Filter inductance & switching frequency both increased to satisfy o/p voltage & current.
  → Switching & Conduction power dissipation of power MOSFETS & filter inductor(↑) .
  → Efficiency degrades (↓).

Cascode OTA (Operational Trans-conductance Amplifier)

for Power Stage of current mode converter

- Control-to-o/p transfer function has real poles
- Pole from o/p filtering capacitor heavily dependent on equivalent resistance of load R_L.
- Poor frequency response.

➤ **Dynamic Response ⇒ Pole-Zero Cancellation Preferred.**

- Band width can be extended.
- Speed up Response time

Tr

$$A(s) = \frac{V_a}{bV_o} \approx g_m R_o \frac{1 + sC_C R_Z}{1 + sC_c R_o}$$

→ , for $R_o >> R_Z$.

where, g_m Trans-conductance of OTA

R_o → O/p resistance of the OTA.

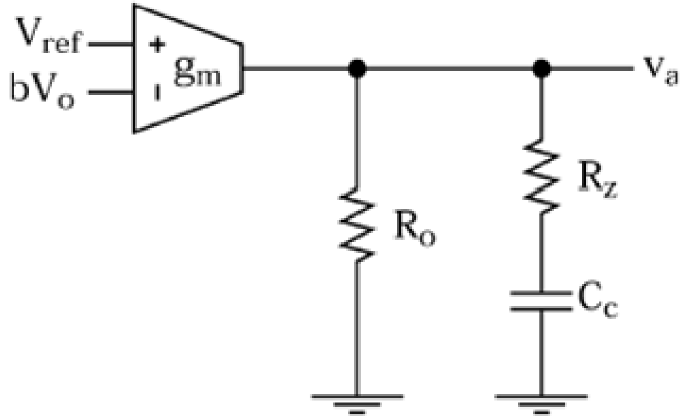


Fig. Schematic of Pole-Zero cancellation Compensator.

Compensator

- g_m & R_o → important for frequency compensation
  → determine gain & phase margin of DC/DC converter
  → depend on biasing current

Result

- Average -20 dB/dec closed loop-gain.
- Sufficient phase margin below unity gain frequency.
- Two Stage OTA → Higher gain
  → Large output swing

Circuit Implementation

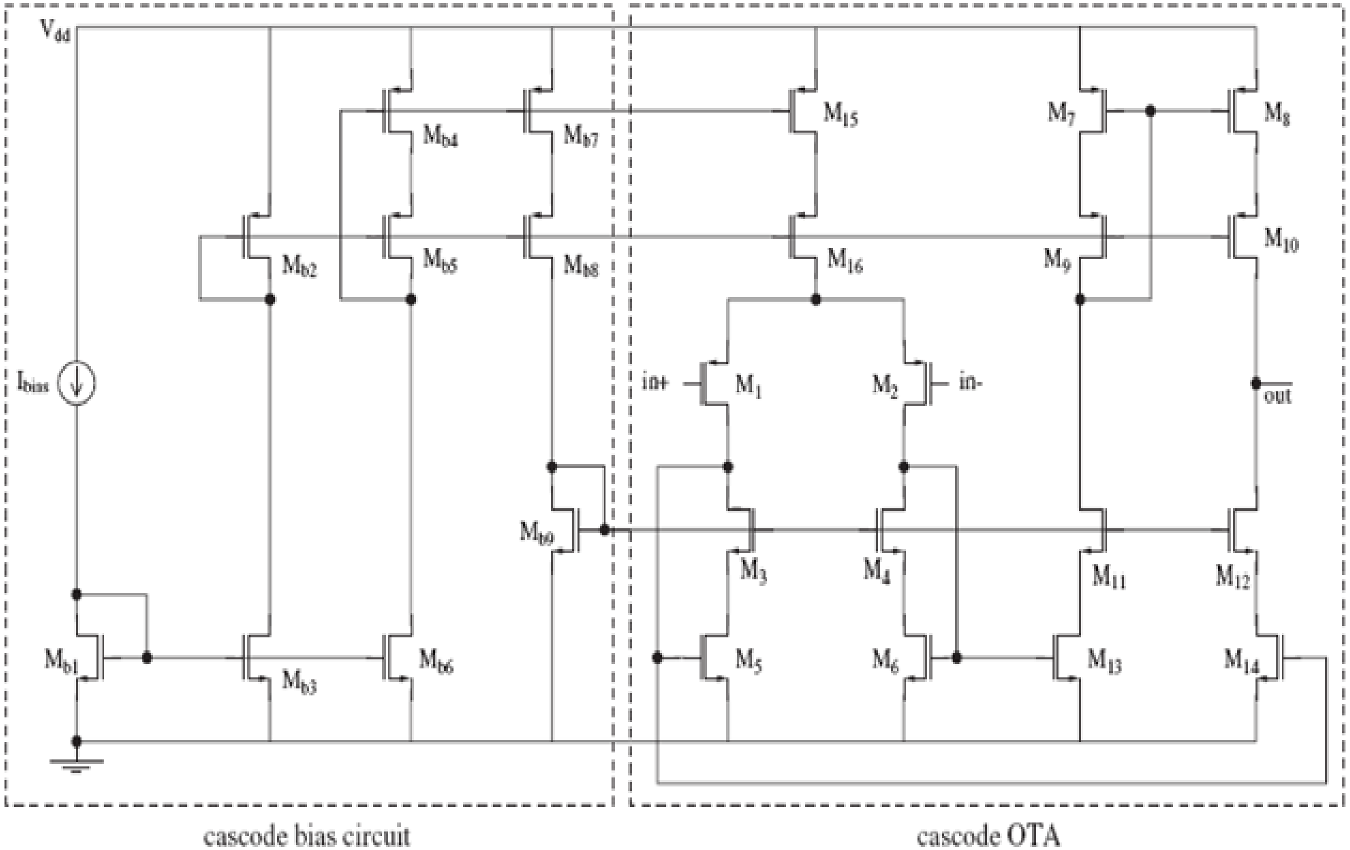


Fig. Schematic of the Cascode OTA.

- ✓Single Stage Amplifier
- ✓High gain & only one dominant pole

On Chip Current Sensing Technique (to Sense Inductor Signal)

- Aspect ratio of M_2 << M_1 in power stage.
- Op amp enforce same voltage at node A & B.
- O/p current I_O flows through M_1.
- Switch MS_1 is shorted.
- $V_{DS}(M_1) = V_{DS}(M_2)$
- I_S (Sensing current) << I_O
- I_2 << I_S
- V_{sense} in control feedback loop
- M_{rs} operate in saturation

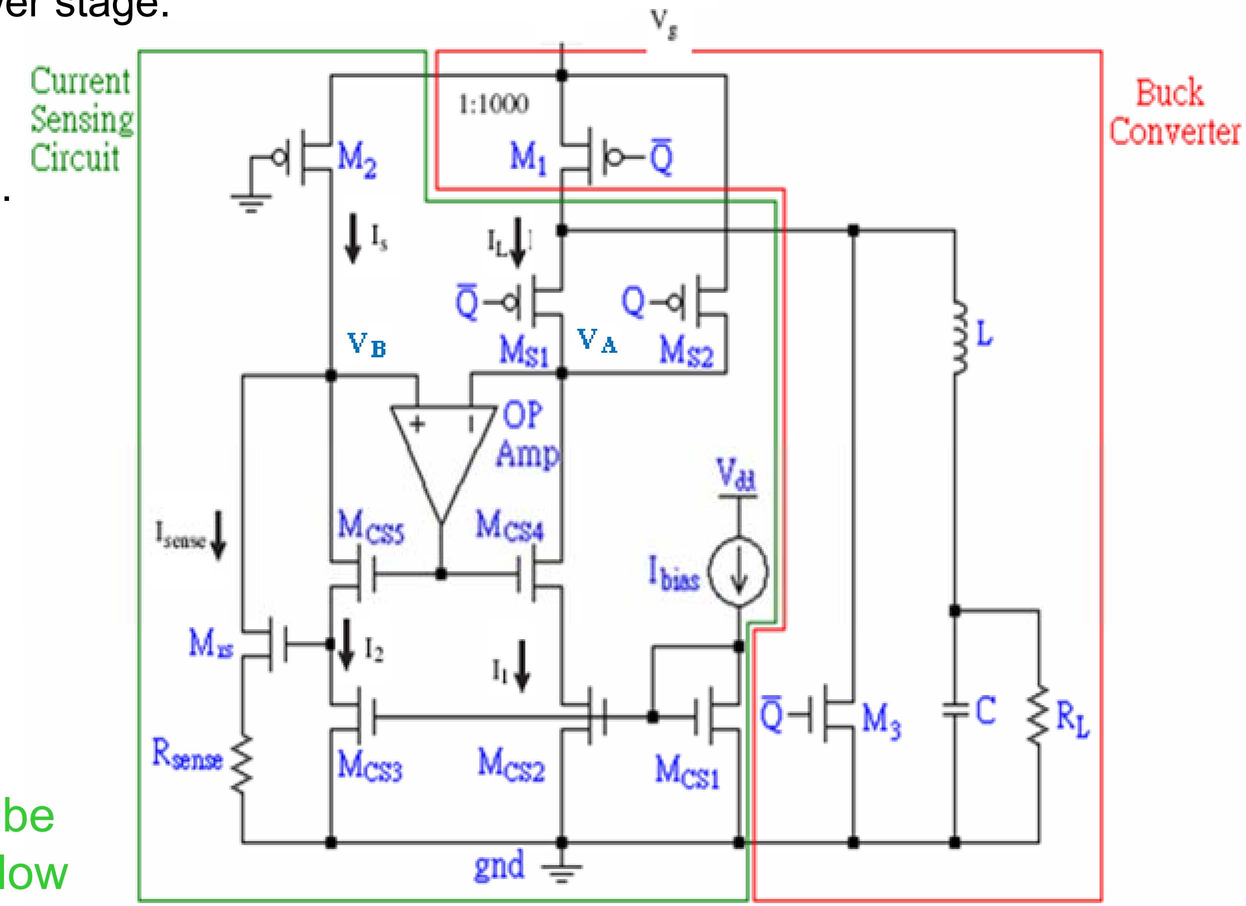


Fig. Schematic of on Chip Current Sensing Circuit.

The sensing scheme needs to be realized with high bandwidth &low power consumption.

Characteristics

- $V_{sense} = I_{sense} R_{sense} = I_L R_{sense} / 1000$
- High gain amplifier required for accurate current sensing.
- Accuracy of sensed current depend on:
  - current mirror M_1 & M_2.
  - On-chip resistor R_{sense}.
- Matching of M_1 & M_2 depend on:
  - Mobility, μ
  - Oxide capacitance, C_{ox}.
  - Threshold voltage, V_T.
  - Location of M_2 to minimize error.

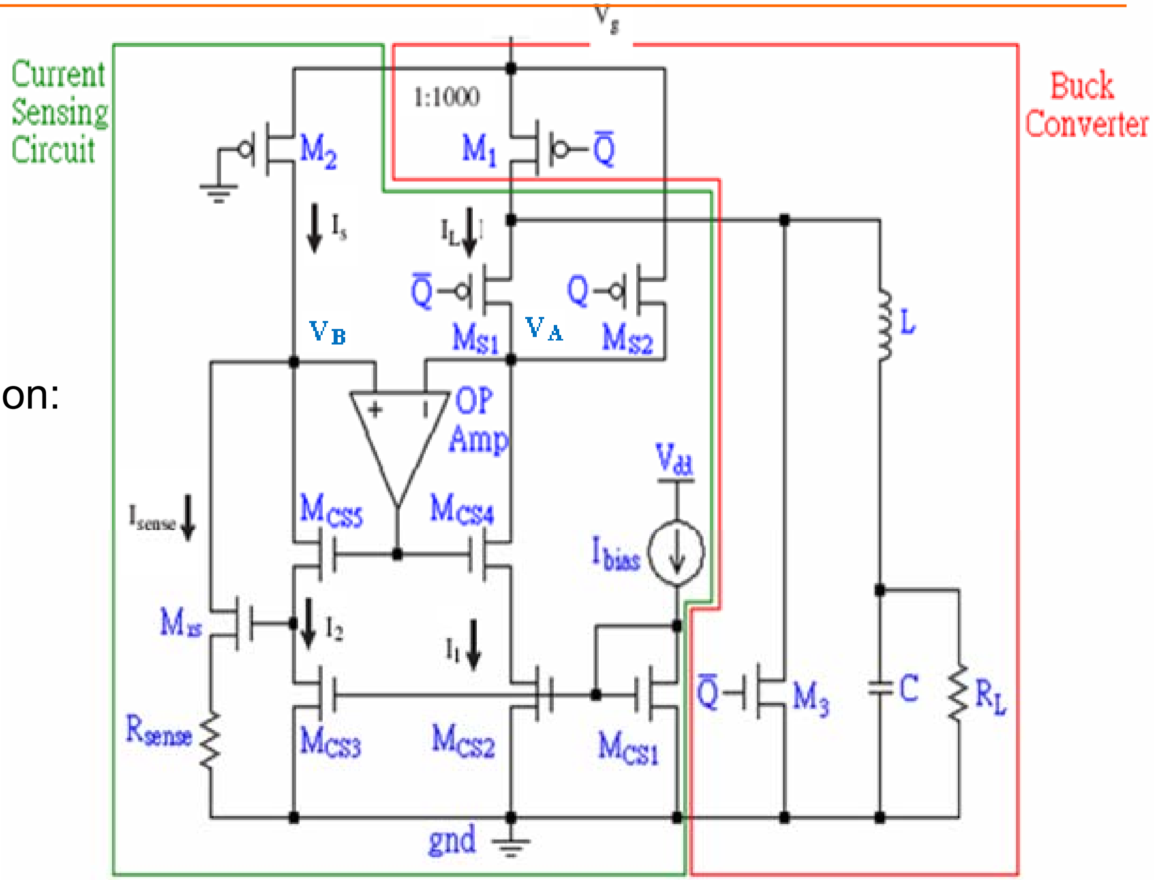


Fig. Schematic of on Chip Current Sensing Circuit.

Advantages

- I_{sense} ⟶ small
  - Hence, power loss reduced in the sensing circuit.
  - Improve efficiency of converter.

On-chip current-sensing circuit can be extended to sense power NMOS transistor by building complementary circuit for other topologies – boost converter & buck-boost converter.

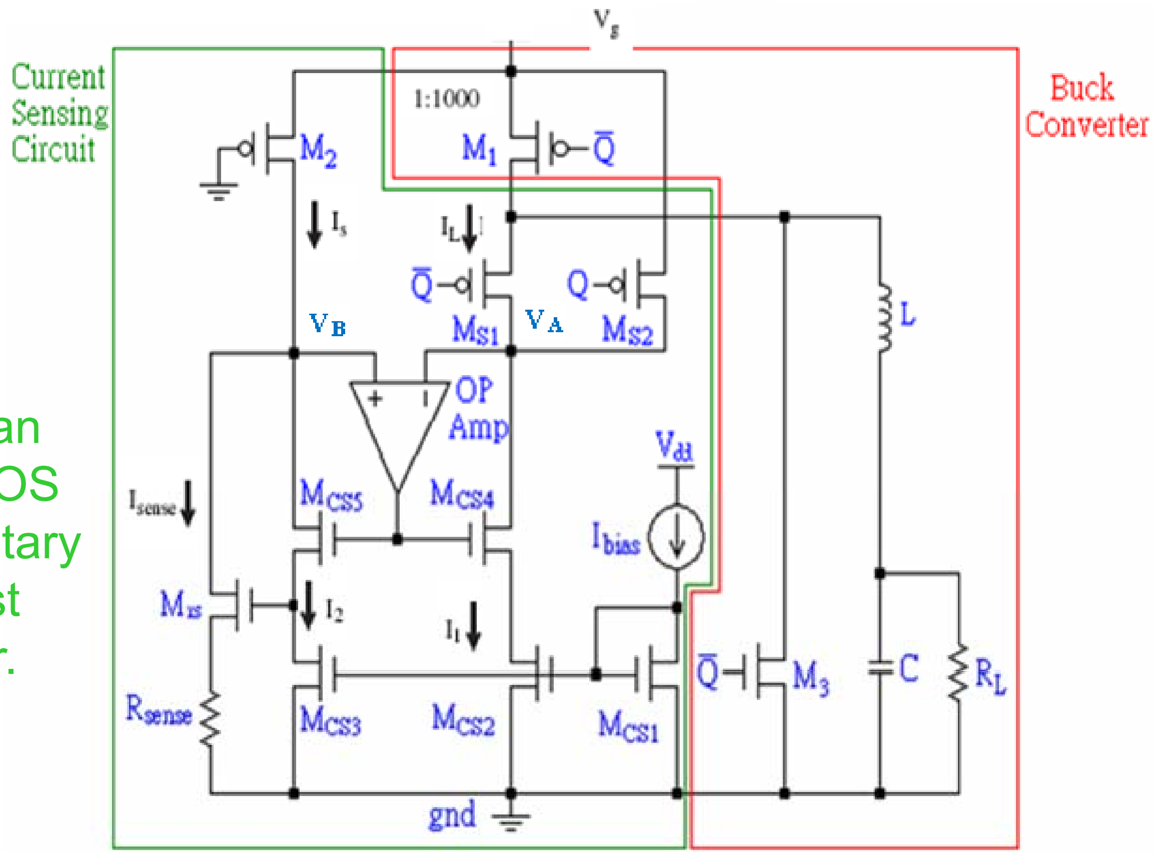


Fig. Schematic of on Chip Current Sensing Circuit.

Comparator

- Needed in both:
  - modulator in feedback control (PWM control).
  - hysteretic comparator in the Oscillator & ramp generator circuit.

- Implemented by a source-coupled differential pair with positive feedback to provide a high gain.
- Gain of positive feedback gain stage is:

$$A_v = \sqrt{\frac{\mu_p (\frac{W}{L})_1}{\mu_n (\frac{W}{L})_2}} \frac{1}{(1-\alpha)}$$

where, $\alpha = \frac{(\frac{W}{L})_5}{(\frac{W}{L})_3}$ is the positive feedback factor.

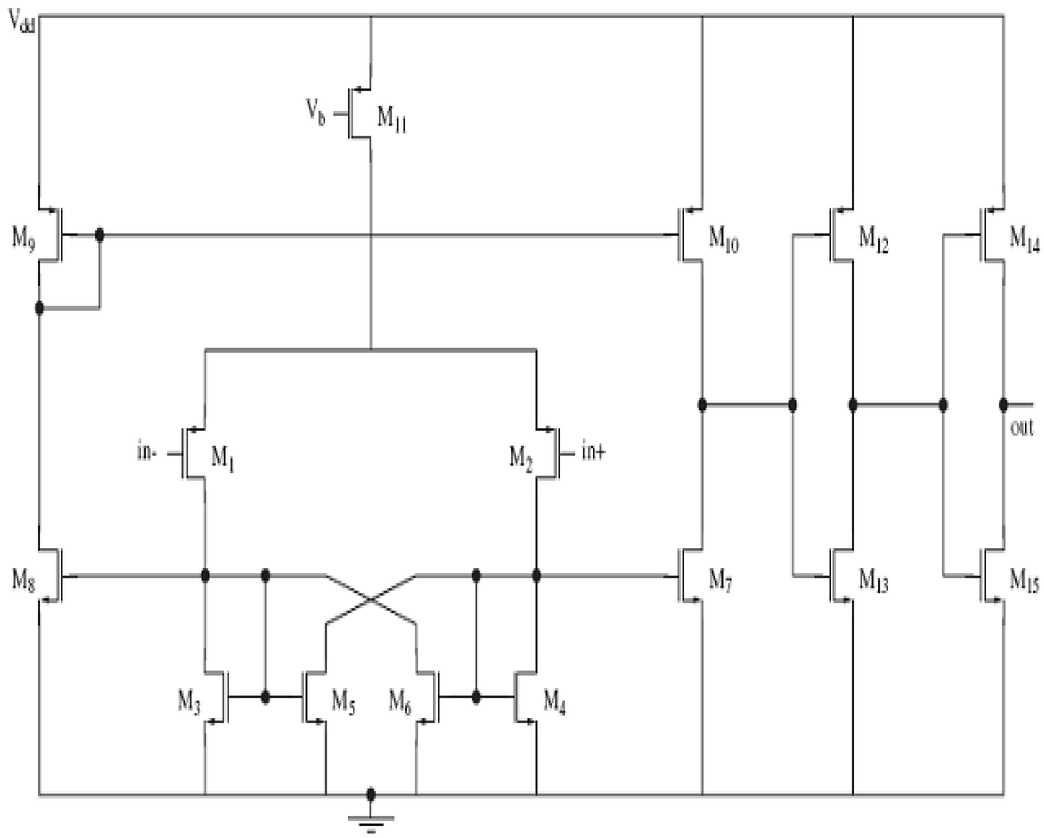


Fig. Schematic of the Comparator.

Comparator

Use of Inverter Chains

- Inverter chains M_{12}-M_{15}
- Increase the response of comparator o/p signal.
- Act as driver stage such that:-
  - M_7 & M_8 can be made smaller.
  - Reduce parasitic capacitance at gates of M_7 & M_8.
  - Results Faster Response.

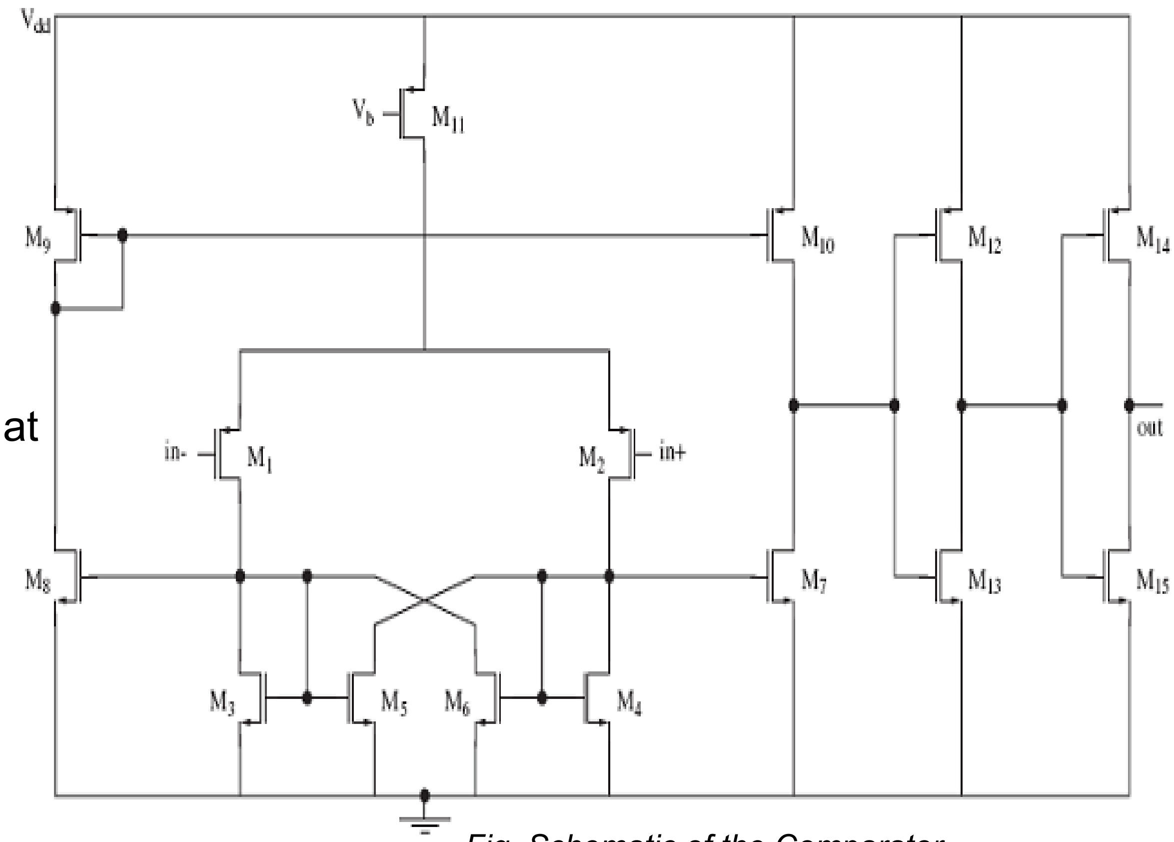


Fig. Schematic of the Comparator.

Simulation:15ns delay time → Adequate for applications with switching frequency of few MHz.

Oscillator and Ramp Generator

- **Used to generate:**
  - . the clock & ramp signals for PWM control.
  - Compensation slope for current mode converter
- **Consists of:**
  - Voltage-to-current(V-I) converter.
  - Hysteretic comparator.
- **Clock frequency & slope of compensation ramp are:**
  - Synchronized with each other.
  - Depend on v_{ref}, C_t, R_t, V_H & V_L.

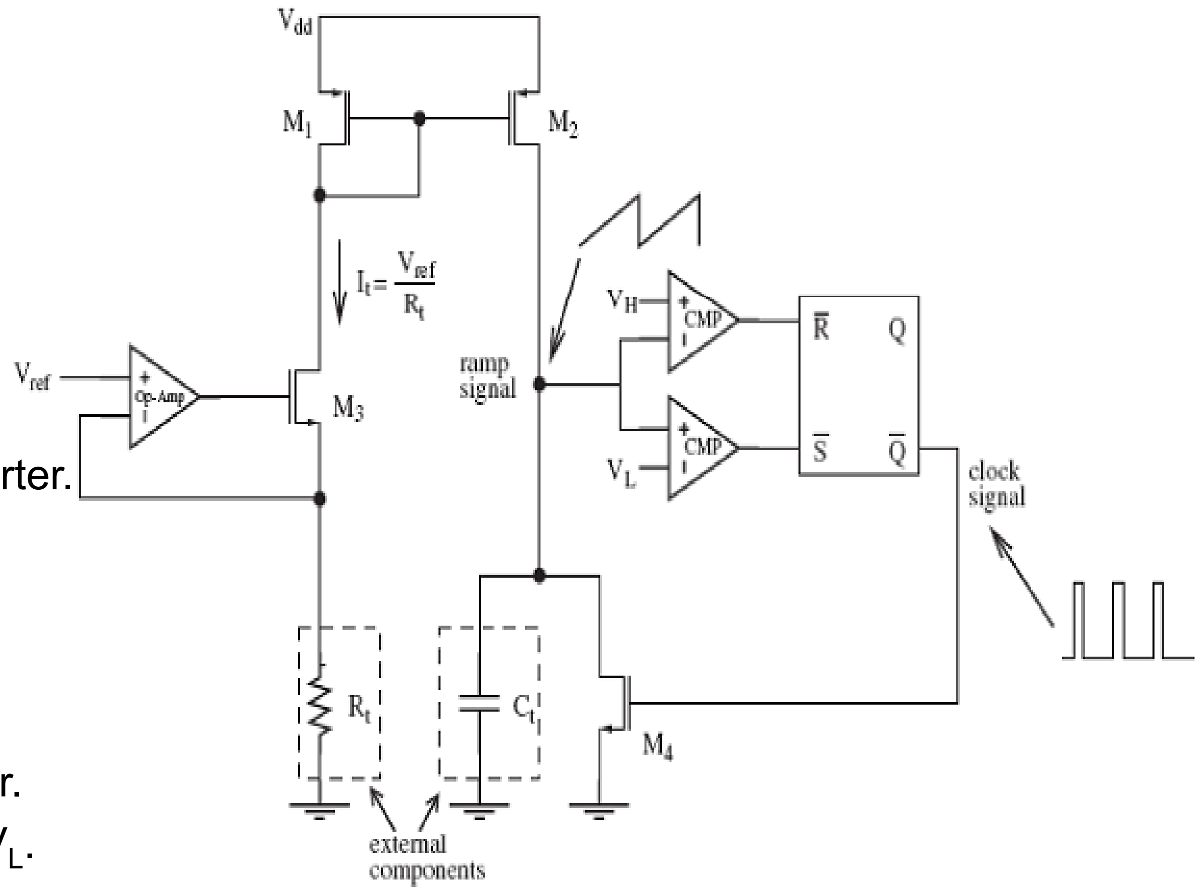


Fig. Schematic of the Oscillator and Ramp Generator.

R_t & C_t can be off-chip components → Switching frequency can be adjusted for different applications.

V-I Converter

- In current mode converters, compensation ramp add with inductor current signal to avoid sub harmonic oscillations.
- V-I designed to convert ramp signal & sensing inductor signal into current.
- V-I converter is a cascade of:
  1. Source follower
  2. Common-source config.
  - I/p voltage of ramp vol.

    & sensing voltage range from 300-1000mV.
  - Not high enough to turn 'ON' M_2 & M_4.

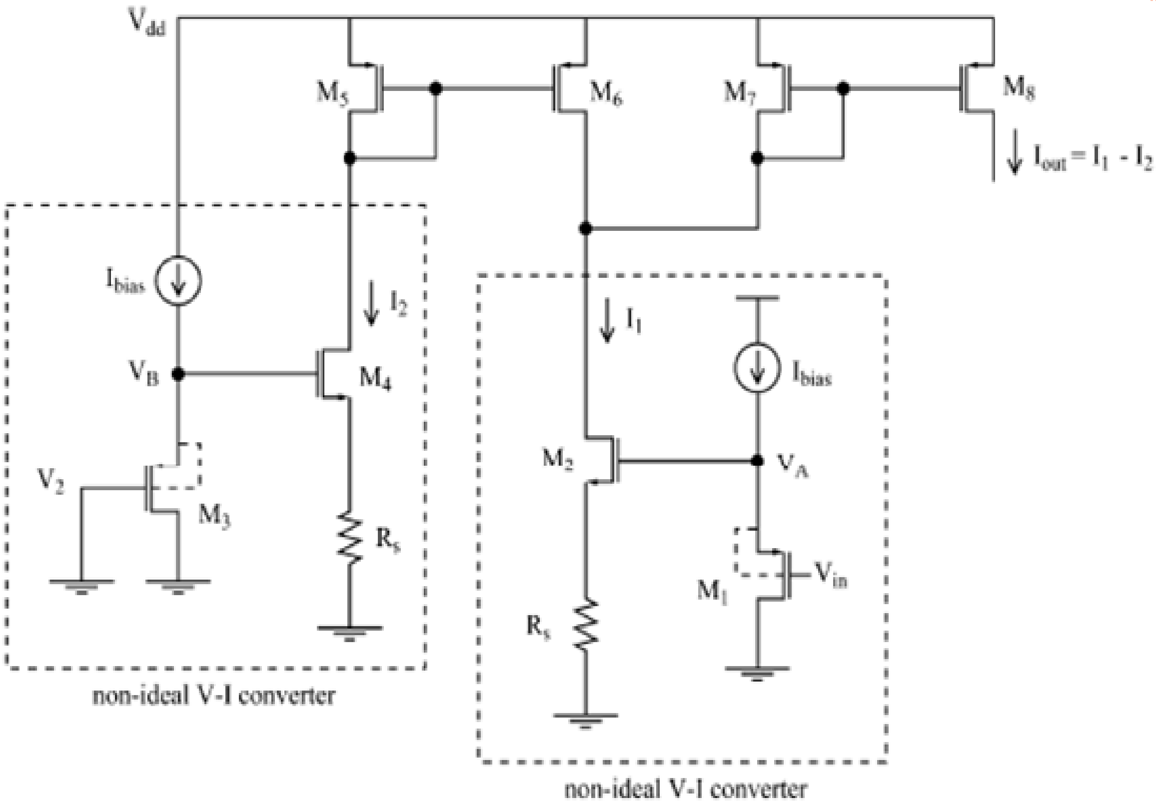


Fig. Schematic of the V – I Converter.

V-I Converter

- Now, $V_A = V_{in} + V_{SG1}$
- For 2[nd] stage V-I converter:

Trans-conductance,

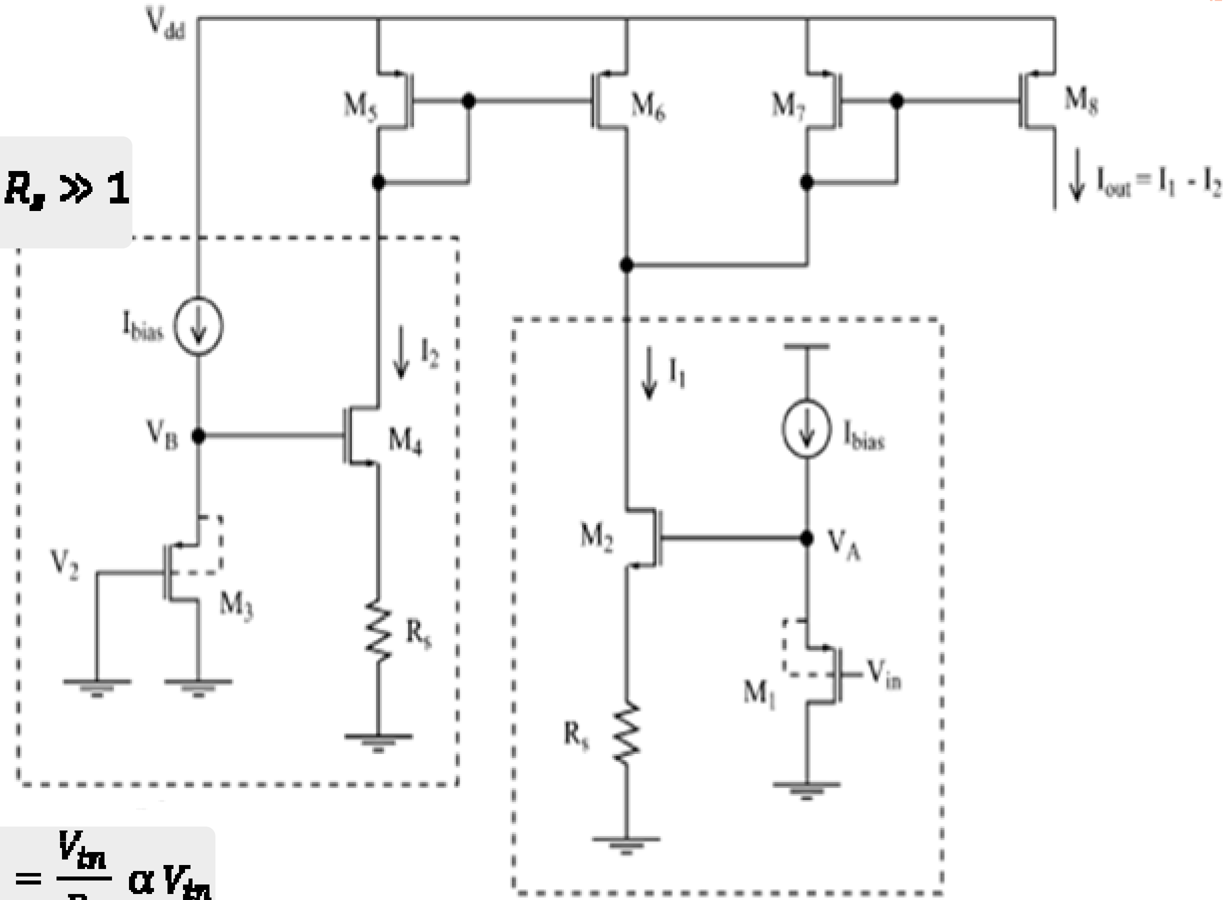
$$G_{m2} = \frac{I_1}{V_A} = \frac{g_{m2}}{1 + g_{m2} R_s} \approx \frac{1}{R_s} \quad for\ g_{m2} R_s \gg 1$$

Then, the o/p current is given by,

$$I_1 = \frac{V_A}{R_s} = \frac{V_{in} + V_{SG1}}{R_s}$$

- Need to eliminate non-ideal term, $\frac{V_{SG1}}{R_S}$
- Now, $I_2 = \frac{V_{SG3}}{R_s}$
- Hence, o/p current I_{out} ,

$$I_{out} = I_1 - I_2 = \left(\frac{V_{in}}{R_s} + \frac{V_{SG3}}{R_s}\right) - \frac{V_{SG1}}{R_s} = \frac{V_{in}}{R_s} \,\alpha\, V_{in}$$



V-I Converter

- Now, sensing voltage, $V_{sense} = I_{sense} R_{sense}$
- Hence, o/p current, I_{out}

$$I_{out} = \frac{V_{sense}}{R_s} = I_{sense}\left(\frac{R_{sense}}{R_s}\right)$$

- I_{out} & I_{sense} do not depend on value of R_s & R_{sense}, rather on the ratio
  - Can be easily controlled.

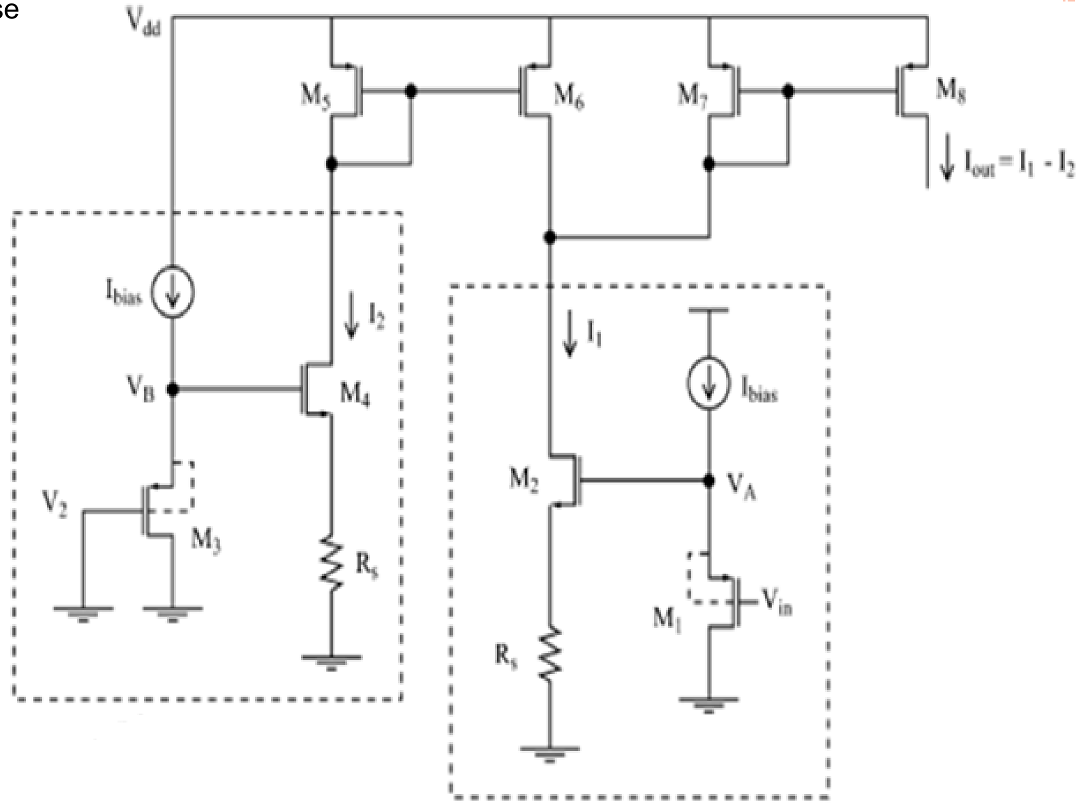


Fig. Schematic of the V – I Converter.

Pulse width Generator

- S=1, R=1 is a forbidden state for the SR Latch.
- At startup, O/p of compensator V_c is low compared with sum of the ramp & sensed signal.
- Hence, R is always High.
- However, the given circuit ensures that RS latch do not reach forbidden state.
- R & S do not go High simultaneously.

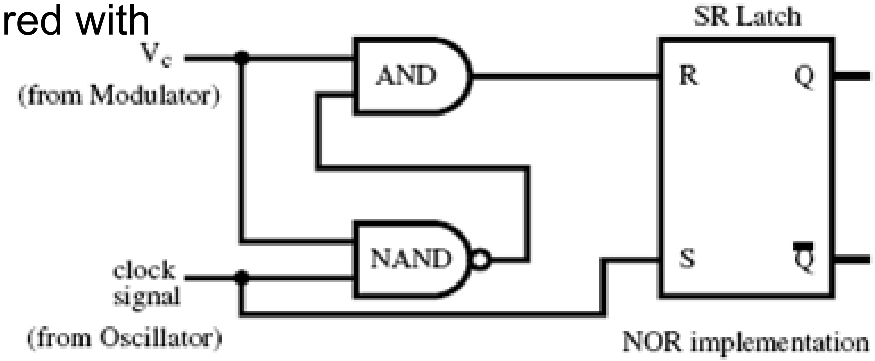


Fig. Schematic of Pulse width Generator.

Buffer

➢ Required for receiving and amplifying the signal produced by the control circuit.

➢Poorly designed buffer with a simple inverter Chain ⟶ a shoot-through current will occur and a large current will pass through the power transistors during each switching transition.

➢Hence, buffer without short-circuit power consumption is needed.

➢Power rails of the buffer should be laid-out carefully & resistances to be minimized So that the converter efficiency do not degrade.

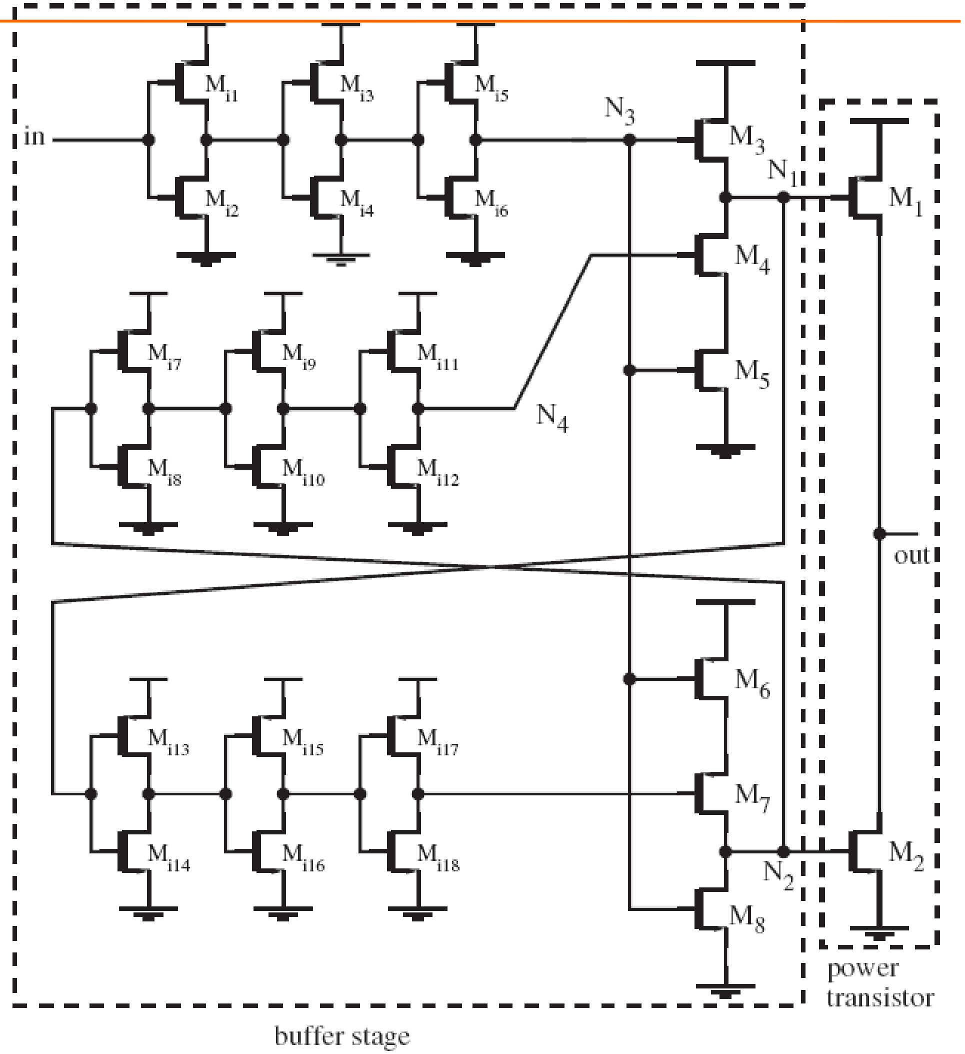


Fig. Schematic of Buffer without short-circuit power consumption.

Power Losses in DC/DC Converter

- **Conduction Loss**
- **Switching Loss**

Related to the size of Power Transistors
❑Optimum Sizing required to improve Efficiency.

- **Shoot through current Loss**

Related to design of buffer Stage to drive power transistors.

- Significant energy dissipated in parasitic impedances of circuit board inter connect & discrete components of the regulator.
- **Conduction Losses:** Caused by the parasitic resistive impedances.
- **Switching Losses:** Due to parasitic capacitive impedances of circuit components.
- Power consumed by PWM feedback circuit & integrated filter capacitor is small as compared to the power consumption of the power train (the power MOSFETs, MOSFET gate drivers, the filter inductor).

- Buck converter O/p, $V_{DD2}(t)=DV_{DD1} + V_{ripple}(t)$.
- Ripple Current, $\Delta i = (V_{DD1} - V_{DD2})D/2Lf_s$.
- Amplitude of voltage ripple,

$$\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})D}{16LCf_s^2} = \frac{\Delta i}{8Cf_s}$$

where, L → Filter inductance.
C → Filter Capacitor.
f_s → Switching frequency.

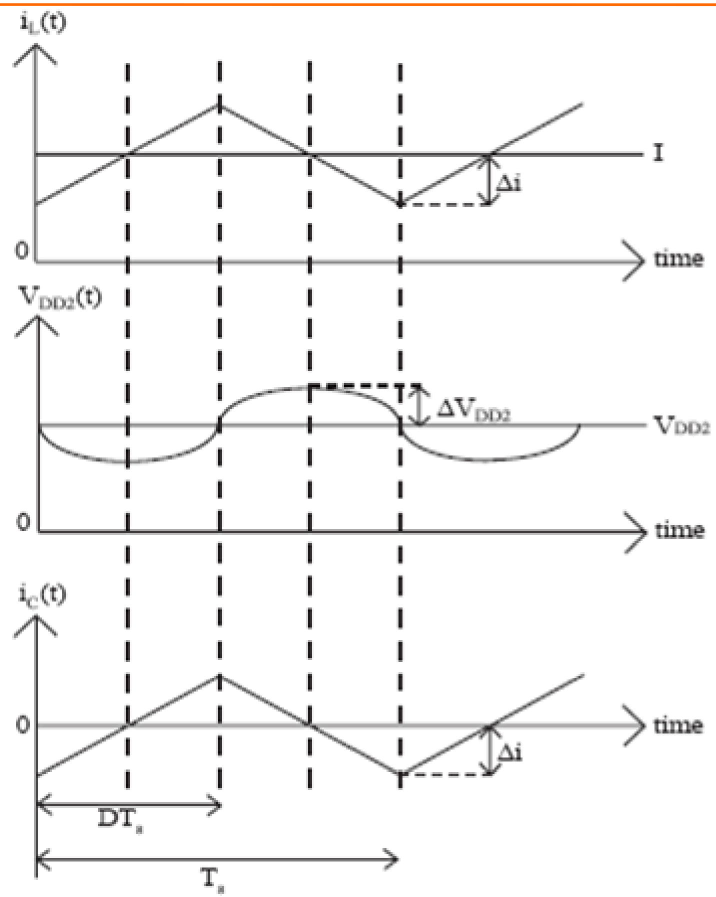


Fig. Inductor Current $i_L(t)$, Output voltage $V_{DD2}(t)$, capacitor current $i_C(t)$ waveforms.

- **MOSEFETs Related Power**
- Combination of Conduction loss & Dynamic Switching loss.
- Conduction power ⟶ Dissipated in series resistance of transistor
- Dynamic Power ⟶ Dissipated in each switching cycle of charging/discharging of Gate oxide, gate-to-source/drain overlap & drain-to-body junction capacitance of MOSFET.
- MOSFET width optimized to minimize power dissipation.
- Optimized power consumption is:

$$P_{tot,MOS}(opt) = a\sqrt{\left(I^2 + \frac{I^2}{3}\right) f_s}$$

$$a = 2\left(\sqrt{R_{oNMOS}(1-D)E_{NMOS}} + \sqrt{R_{oPMOS} D E_{PMOS}}\right)$$

$$E = 2(C_{ox} + C_{gs} + 2C_{gd} + C_{db})V_{DD1}^{2}$$

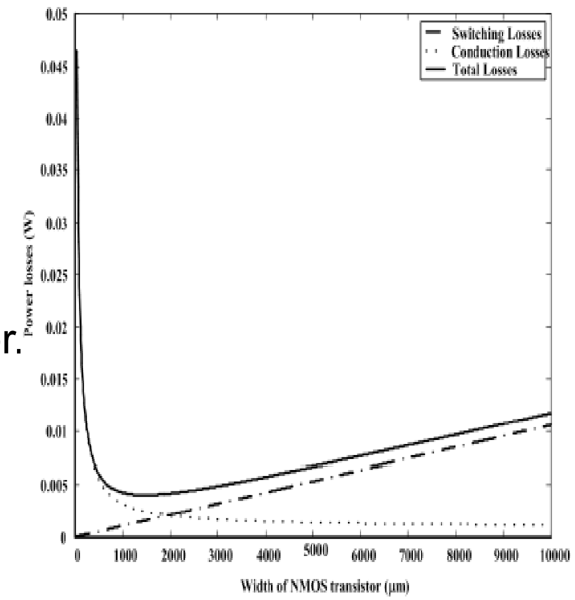
Where, R_o ⟶ equivalent series resistance of a 1µm wide transistor.

C_{ox} ⟶ gate oxide capacitance.

C_{gs} ⟶ gate-to-source overlap.

C_{gd} ⟶ gate-to-drain overlap.

C_{db} ⟶ drain-to-body junction capacitance.



- **Filter Inductor Power**
- Energy consumption due to:
  - Series resistance of filter inductor.
  - Stray capacitance of filter inductor.
- Total power consumption in inductor is:

$$P_{tot,inductor} = b\left(\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{Lo} {V_{DD1}}^2}{R_{Lo} \Delta i}\right)$$

$$b = \frac{(V_{DD1} - V_{DD2}) D R_{Lo}}{2}$$

Where, C_{Lo} → Parasitic stray capacitance per nH Inductance.

R_{Lo} → Parasitic Series Resistance per nH Inductance.

- **Filter Capacitor Related Power**
- Integrated Capacitor implemented utilizing Gate Oxide Capacitance of MOSFET
- Total Power dissipation of a filter Capacitor is:

$$P_{tot,capacitor} = d f_s \Delta I$$

$$d = \frac{8 R_{ocap} L_{cap} C_o \Delta V_{DD2}}{3}$$

Where, R_{ocap} ⟶ Series Capacitance of MOSFET with 1µm width.

C_o ⟶ Gate Oxide Capacitance per µm^2.

L_{cap} ⟶ Channel Length of the MOSFET.

- **Total Power Consumption of Buck Converter**

$$P_{buck} - P_{tot,MOS}(opt) + P_{tot,inductor} + P_{tot,capacitor}$$

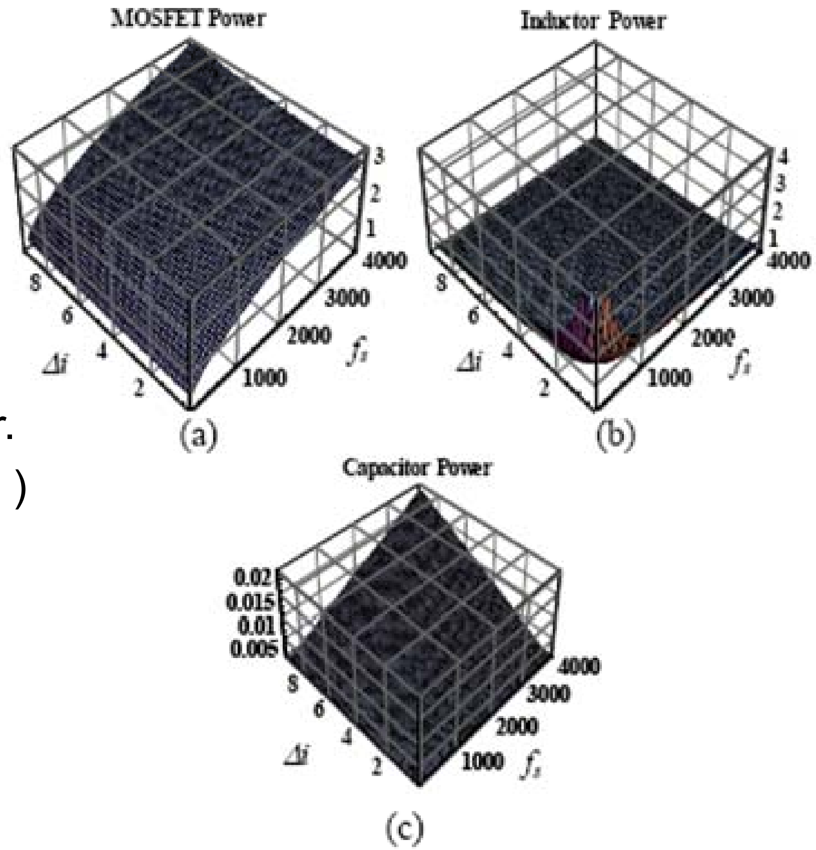
$$P_{buck} = a\sqrt{\left(I^2 + \frac{i^2}{3}\right)} f_s + b\left(\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{Lo} {V_{DD1}}^2}{R_{Lo}\,\Delta i}\right) + d f_s \Delta i$$

- Strongly function of Switching frequency (f_s) & Ripple Current (Δi).
- $P_{tot,\ capacitor}$ (↑) → As f_s & Δi (↑).
- $P_{tot,\ inductor}$ (↓) → As f_s & Δi (↑).
- $P_{tot,\ capacitor}$ → Negligibly small (less than 1%) as compared to Inductor & MOSFET Power.

- **Efficiency, η**

$$\eta = 100 * \frac{P_{Load}}{P_{Load} + P_{buck}}$$

$$P_{buck} = a\sqrt{\left(I^2 + \frac{i^2}{3}\right) f_s} + b\left(\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{Lo} V_{DD1}^2}{R_{Lo} \Delta i}\right) + d f_s \Delta i$$



- Low f_s & Δi ⟶ Power dissipation mainly in the Inductor.
- As f_s & Δi (↑) ⟶ Inductor Loss (↓) (Parasitic Loss ↓)
  MOSFET Power Loss (↑)
- As Inductor loss dominate ⟶ Loss (↓)

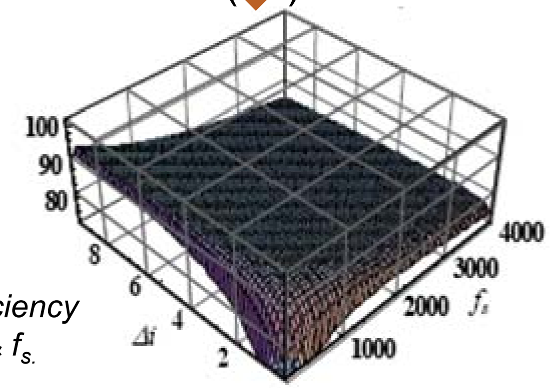


Fig. Converter Efficiency as functions of Δi & f_s.

Fig. (a) MOSFET Power (b) Inductor Power (c) Capacitor Power as functions of Δi & f_s.

Δi in Amps & f_s in MHz .

Efficiency Analysis

As the filter capacitance (↓) ⟶ The filter inductance & switching frequency are both (↑) to satisfy the output voltage and current requirements.

⟶ Both the switching and conduction power dissipation of the power MOSFETs and the filter inductor increases.

⟶ thereby degrading the efficiency.

Major challenges for a monolithic switching DC-DC converter

- The area occupied by the integrated filter capacitor.
- The effect of the parasitic impedance characteristics of the integrated inductors on the overall efficiency characteristics of a switching DC-DC converter.

Light Load Efficiency in DC/DC Converter (to Improve Efficiency)

- Battery-powered portable electronic devices like cell phones, Laptops etc.
- Full loading not present for prolonged periods.
- Rather devices run at light loads (Stand-By mode) for most of the time.
- **Region I**
  - Conduction Losses dominate.
- **Region II**
  - Switching Losses proportional to load Current, i/p voltage, switching frequency.
- **Region III**
  - Gate-drive losses while charging/discharging Gate Capacitances of Power transistors during Switching transition.

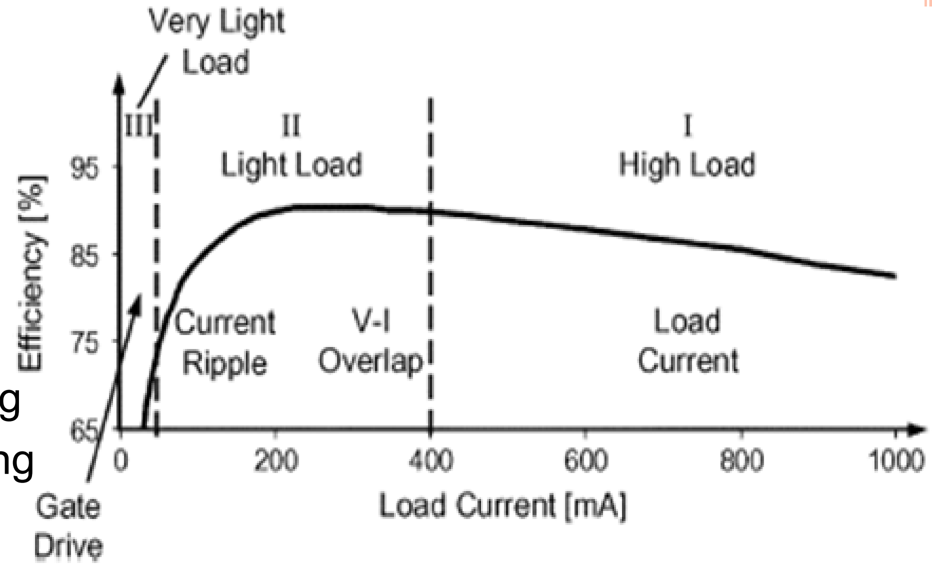


Fig. Efficiency Curve of DC/DC Converter.

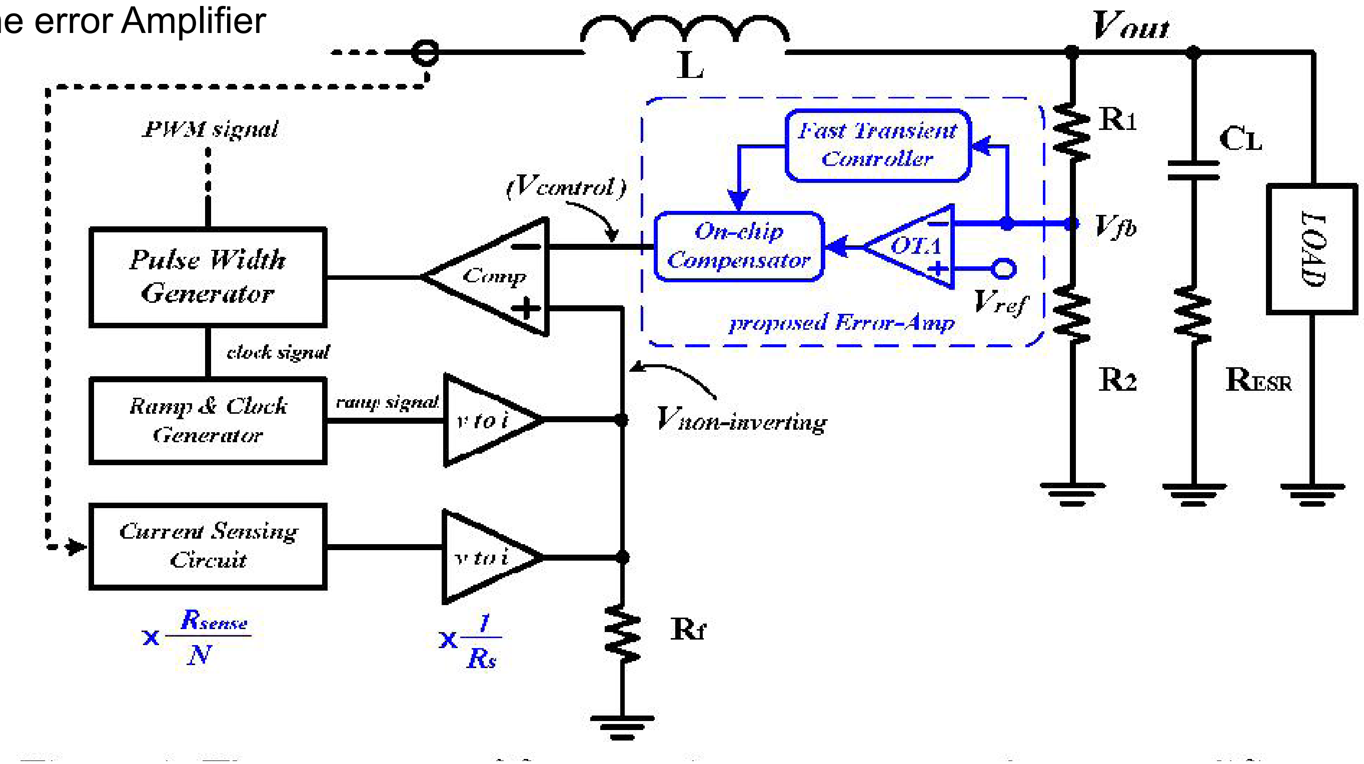
Decreasing Switching Frequency ⟹ Best way to Reduce Total Loss.

Compensated Error Amplifier (for Fast Transient Response)

- Fast transient response of o/p voltage reveals critical point for large load variations.
- Required to supply reliable voltage.

Solution

- Large Transconductance for the error Amplifier For large load variations.
- Uses on-chip current mode Milller capacitor (replaces large Off capacitor).
- Decrease transient response Time.



Compensated Error Amplifier (for Fast Transient Response)

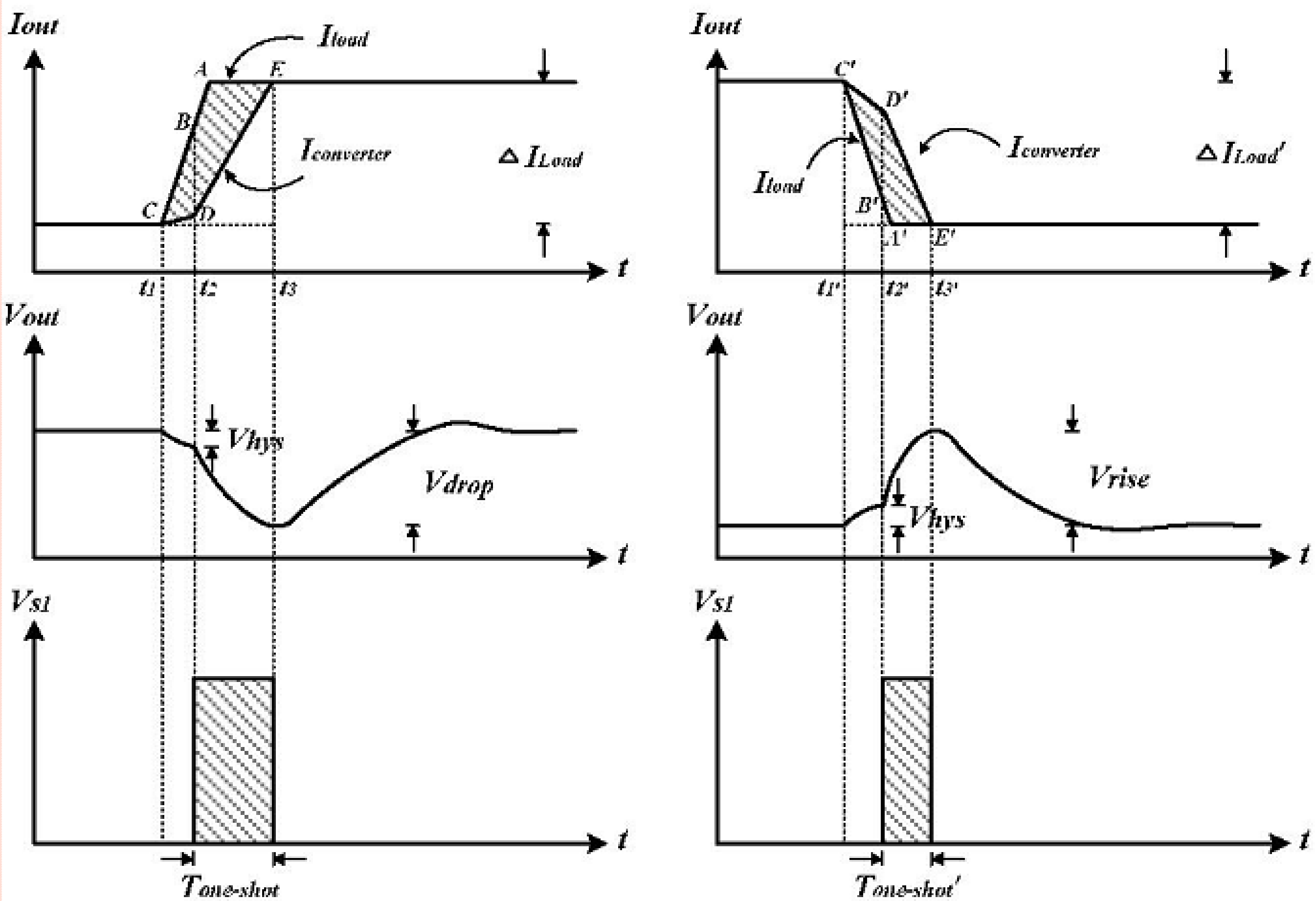


Fig. Timing Analysis of signal waveforms. (a) With a positive & sudden load variation. (b) With a negative & sudden load current variation.

- Better Response Time.

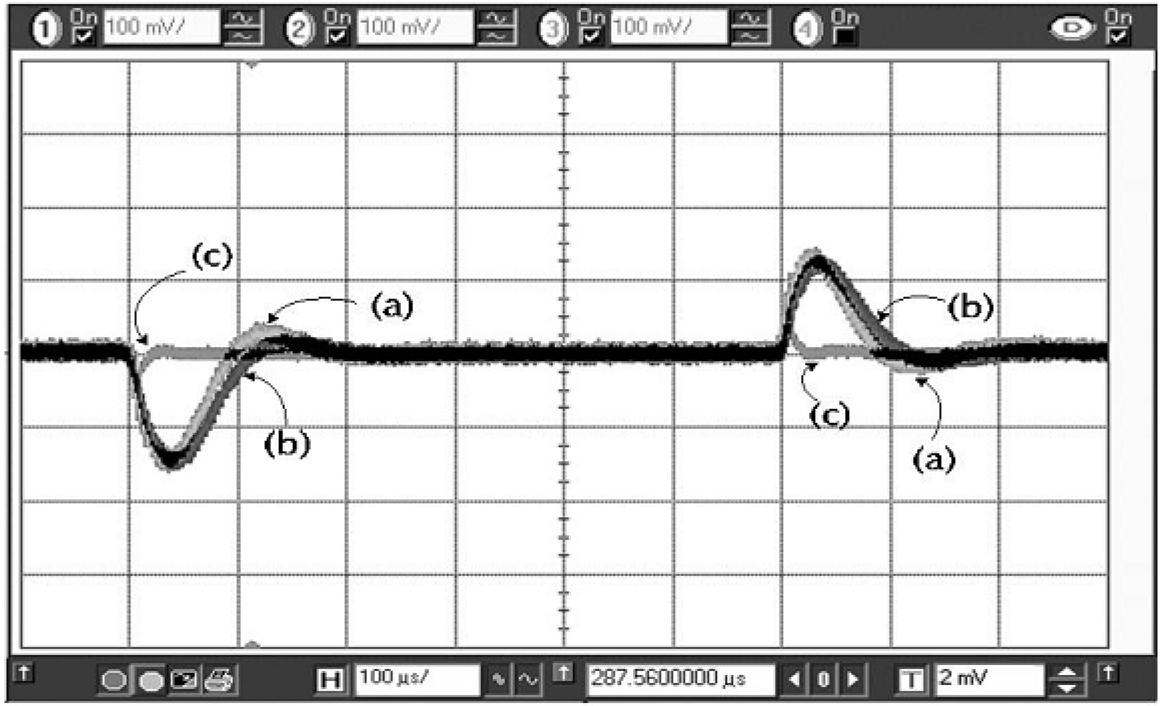


Fig. The transient response with load current step b/w 100mA & 400mA. (a) Conventional error amplifier. (b) On-chip compensated error amplifier without fast transient controller. (c) On-chip compensated error amplifier with fast transient controller.

Issues with Monolithic DC/DC Converters

- High Efficiency with large input voltage range.
- High Performance System-on-chip (SOC) systems
- Dynamic Power Management
- Fast Dynamic Response
- Low Power Consumption: low stand by power.
- Need to provide robust Output Voltage regulation
- Maximum Efficiency
- Minimize Ripple noise on Input & Output
- Minimize cost
- To have accurate sensed current for current mode PWM controller
- Reduce supply voltage demand, greater amount of current from external power supplies .
- Voltage scaling capability.

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Questions???

THANK YOU !!!